In the Claims:

1. (Cancelled)

2. (Previously presented) Level shifting circuitry, comprising:

a level-shifting section responsive to an input logic signal, such input logic signal having a first voltage level representative of a first logic state or a second voltage level representative of a second logic state, such level-shifting section providing an output logic signal at an output terminal thereof having a third voltage level representative of the first logic state of the input logic signal; and a fourth voltage level representative of the second logic state of the input signal;

an enable/disable section coupled to the level shifting section, the enable/disable section being responsive to an enable/disable signal, the enable/disable section placing the output terminal at a relatively high output impedance condition independent of the logic state of the input logic signal during a disable mode;

wherein the level-shifting circuitry includes:

an input transistor having a control electrode, a first electrode coupled to the input logic signal, and a second electrode;

a first switching transistor;

a second switching transistor;

an output pair of serially coupled complementary type transistors, a first one of the pair of transistors having a first electrode coupled to a source of the third voltage level through the first switching transistor and a control electrode coupled to the second electrode of the input transistor, a junction between the output pair of transistors providing the output terminal for the

level-shifting circuitry, a control electrode of the second one of the pair of transistors being connected to the second electrode of the input transistor, the second one of the pair of transistors having a second electrode coupled to the fourth voltage level through the second switching transistor; and

wherein the first and second switching transistors are fed by the enable/disable signal.

3. (Previously presented) The level shifting circuitry recited in claim 2 wherein the enable/disable section includes an inverter, and wherein such inverter is fed by the enable/disable signal, such inverter having an output coupled to the control electrode of the first switching transistor.

4. (Previously presented) The level shifting circuitry recited in claim 3 wherein the inverter is powered by a voltage source held at the first voltage level.

5. (Original) The level shifting circuitry recited in claim 4 wherein the control electrode of the input transistor is coupled to the source of the first voltage level.

6. (Previously presented) Level shifting circuitry comprising:

a level-shifting section responsive to an input logic signal, such input logic signal having a first voltage level representative of a first logic state or a second voltage level representative of a second logic state, such level-shifting section providing an output logic signal at an output terminal thereof having a third voltage level representative of the first logic state of the input logic signal;

an enable/disable section coupled to the output terminal, the enable/disable section being responsive to an enable/disable signal, the enable/disable section placing the output terminal at a relatively high output impedance condition independent of the logic state of the input logic signal during a disable mode, the enable/disable section including a first switching transistor and a second switching transistor;

wherein the level-shifting section includes:

an input transistor having a control electrode, a first electrode coupled to the input logic signal, and a second electrode;

an output pair of serially coupled complementary type transistors, a first one of the pair of transistors having a first electrode coupled to a source of the third voltage level through the first switching transistor and a control electrode coupled to the second electrode of the input transistor, a junction between the output pair of transistors providing the output terminal for the level-shifting circuitry, a control electrode of the second one of the pair of transistors being connected to the second electrode of the input transistor, the second one of the pair of transistors having a second electrode coupled to the second voltage level through the second switching transistor;

wherein the first and second switching transistors are fed by the enable/disable signal;

wherein the enable/disable section includes an inverter, and wherein such inverter is fed by the enable/disable signal, such inverter having an output coupled to the control electrode of the first switching transistor;

wherein the inverter is powered by a source of the first voltage level; and

wherein the inverter comprises a level shifter for shifting the level of the enable/disable signal from the first voltage level to the third voltage level and for feeding such third voltage

level to the control electrode of the first switching transistor to place the first switching transistor to a non-conducting condition during the disable mode.

7. (Previously presented) The level shifting circuitry recited in claim 2 and further comprising an additional transistor having a control electrode coupled to the junction, a first electrode coupled to the source of the third voltage level through the first switching transistor and a second electrode coupled to the second electrode of the input transistor.

8. (Previously presented) The level shifting circuitry recited in claim 7 wherein the input transistor and the additional transistor are of opposite conductivity type.

9. (Currently Amended) A level shifting circuit comprising:

a first reference voltage node carrying a voltage at a first voltage level;

a second reference voltage node carrying a voltage at a second voltage level, the second voltage level being different ~~that the~~ than a first voltage level;

a third reference voltage node carrying a voltage at a third voltage level, the third voltage level being different ~~that~~ than the first voltage level and the second voltage level;

an input node to receive an input signal, the input signal varying between the first voltage level and the second voltage level;

a first n-channel transistor having a first source/drain region, a second source/drain region and a gate, the gate being coupled to the input node;

a second n-channel transistor having a first source/drain region coupled to the second source/drain region of the first n-channel transistor, a second source/drain region coupled to the

second voltage level reference node and a gate coupled to a first enable signal node;

a first p-channel transistor having a first source/drain region coupled to the first source/drain region of the first n-channel transistor, a second source/drain region and a gate coupled to the input node;

a second p-channel transistor having a first source/drain region coupled to the second source/drain region of the first p-channel transistor, a second source/drain region coupled to the third reference node and a gate coupled to a second enable signal node.

10. (Previously Presented) A level shifting circuit comprising:

an input node to receive an input signal, the input signal varying between a first voltage level and a second voltage level;

a first n-channel transistor having a first source/drain region, a second source/drain region and a gate, the gate being coupled to the input node;

a second n-channel transistor having a first source/drain region coupled to the second source/drain region of the first n-channel transistor, a second source/drain region coupled to a second voltage level reference node and a gate coupled to a first enable signal node;

a first p-channel transistor having a first source/drain region coupled to the first source/drain region of the first n-channel transistor, a second source/drain region and a gate coupled to the input node;

a second p-channel transistor having a first source/drain region coupled to the second source/drain region of the first p-channel transistor, a second source/drain region coupled to a third reference node and a gate coupled to a second enable signal node, the third reference node carrying a third voltage level, the third voltage level being different than the first voltage level;

and

a third n-channel transistor having a first source/drain region coupled to the input node, a second source/drain region coupled to the gate of the first p-channel transistor, and a gate coupled to a first voltage level reference node.

11. (Previously presented) The circuit of claim 10 and further comprising a third p-channel transistor having a first source/drain region coupled to the gate of the first p-channel transistor, a second source/drain region coupled to the second source/drain region of the first p-channel transistor, and a gate coupled to the first source/drain region of the first p-channel transistor.

12. (Previously presented) The circuit of claim 11 and further comprising an inverter having an input and an output, the input coupled to the first enable signal node and the output coupled to the second enable signal node.

13. (Previously presented) The circuit of claim 12 wherein the inverter comprises:

a fourth n-channel transistor with a first source/drain region coupled to the second enable signal node, a second source/drain region coupled to the first voltage level reference node, and a gate coupled to the first enable signal node;

a fourth p-channel transistor with a first source/drain region coupled to the second enable signal node, a second source/drain region coupled to the third reference voltage node, and a gate coupled to the first enable signal node.

14. (Previously presented) The circuit of claim 13 wherein the inverter further comprises:

a fifth n-channel transistor with a first source drain region coupled to the first enable signal node, a second source/drain region coupled to gate of the fourth p-channel transistor, and a gate coupled to the first voltage level reference node; and

a fifth p-channel transistor with a first source/drain region coupled to the gate of the fourth p-channel transistor, a second source/drain region coupled to the third reference voltage node, and a gate coupled to first source/drain region of the fourth p-channel transistor.

15. (Previously presented) The circuit of claim 9 wherein a signal carried at the first enable signal node is an inverted version of a signal carried at the second enable signal node.

16. (Currently Amended) A ~~The~~ level shifting circuit ~~of claim 9 and further~~ comprising:

a second reference voltage node carrying a voltage at a second voltage level, the second voltage level being different than a first voltage level;

a third reference voltage node carrying a voltage at a third voltage level, the third voltage level being different that the first voltage level and the second voltage level;

an input node to receive an input signal, the input signal varying between the first voltage level and the second voltage level;

a first n-channel transistor having a first source/drain region, a second source/drain region and a gate, the gate being coupled to the input node;

a second n-channel transistor having a first source/drain region coupled to the second source/drain region of the first n-channel transistor, a second source/drain region coupled to the second voltage level reference node and a gate coupled to a first enable signal node;

a first p-channel transistor having a first source/drain region coupled to the first

source/drain region of the first n-channel transistor, a second source/drain region and a gate coupled to the input node;

a second p-channel transistor having a first source/drain region coupled to the second source/drain region of the first p-channel transistor, a second source/drain region coupled to the third reference node and a gate coupled to a second enable signal node; and

an inverter coupled between the first enable signal node and the second enable signal node, the inverter including a level shifting circuit.

17. (Previously presented) The circuit of claim 16 wherein the inverter includes an input coupled to the first enable signal node and an output coupled to the second enable signal node.

18. (Previously presented) The circuit of claim 9 wherein the third voltage level is greater than the first voltage level.

19. (Previously presented) The circuit of claim 16 wherein the third voltage level is 2.5 volts and the first voltage level is 2.1 volts.

20. (Previously presented) A level shifting circuit comprising:

a level-shifting section responsive to an input logic signal, the input logic signal varying between a first voltage level and a second voltage level, the level-shifting section providing an output logic signal at an output terminal thereof, the output logic signal varying between the first voltage level and a third voltage level, the third voltage level being different than the second voltage level;

a first reference voltage node carrying a voltage at the first voltage level;

a third reference voltage node carrying a voltage at the third voltage level; and

an enable/disable section including a first portion coupled between the level shifting section and the first reference voltage node and a second portion coupled between the level shifting section and the third reference voltage node, the enable/disable section being responsive to an enable/disable signal, the enable/disable section causing the output terminal to be placed at a relatively high output impedance condition independent of the logic state of the input logic signal in response to a disable mode indication from the enable/disable signal.

21. (Currently Amended) The circuit of claim 20 wherein the first voltage level and the third voltage ~~levels~~ level are representative of a first logic state and wherein the first voltage level and the second voltage level [[is]] are representative of a second logic state.

22. (Previously presented) The circuit of claim 20 wherein the level-shifting section comprises:

a first transistor with a current path coupled between the third reference voltage node and the output terminal; and

a second transistor with a current path coupled between the output terminal and the first reference voltage node.

23. (Previously presented) The circuit of claim 22 wherein the enable/disable section comprises:

a third transistor with a current path coupled in series the current path of the first

transistor, the current path of the third transistor coupled between the third reference voltage node and the first transistor; and

a fourth transistor with a current path coupled in series the current path of the second transistor, the current path of the fourth transistor coupled between the first reference voltage node and the second transistor.

24. (Previously presented) The circuit of claim 23 wherein both the third and fourth transistors are rendered conductive when the enable/disable signal indicates that the level shifting circuit is in an enable mode and wherein both the third and fourth transistors are rendered non-conductive when the enable/disable signal indicates that the level shifting circuit is in the disable mode.

25. (Previously presented) The circuit of claim 20 wherein the first portion of the enable/disable section comprises a first switch between the level shifting section and the first reference voltage node and wherein the second portion of the enable/disable section includes a second switch coupled between the level shifting second and the third reference voltage node.

26. (Previously presented) The circuit of claim 25 and further comprising an inverter coupled between a control terminal of the first switch and a control terminal of the second switch.

27. (Previously presented) The circuit of claim 26 wherein the inverter includes an input coupled to the control terminal of the first switch and an output coupled to the control terminal

of the second switch.

28. (Previously presented) The circuit of claim 26 wherein the inverter is coupled to the third reference voltage node.

29. (Previously presented) The circuit of claim 28 wherein the inverter includes a level shifter coupled to the third reference voltage node and to a voltage node at the first voltage level.

30. (Previously presented) The circuit of claim 25 wherein the first and second switches comprise MOS transistors.